REMARKS

New claims 44-59 have been added. No new matter has been added. Support for the new claims is found in at least Figure 3 of the present application. Thus, claims 1-12 and 44-59 are pending in the present application. In the Office Action, claims 1-2 and 4-12 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Jang, et al (U.S. Patent No. 6,049,137). Claim 3 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Jang in view of Ridinger (U.S. Patent No. 4,724,219). The Examiner's rejections are respectfully traversed.

With regard to independent claim 1, Applicants describe and claim providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. For example, Applicants describe forming a silicon-on-insulator (SOI) structure including a silicon substrate, a silicon dioxide insulating layer, and an epitaxial silicon semiconductor layer. See Patent Application, page 10, ll. 21-24 and Figure 1. Applicants further describe and claim forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate, and forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate. Applicants also describe and claim forming a layer of material above the alignment mark and in the opening.

In contrast, Jang is concerned with layers of material that are formed over alignment targets on a wafer. The overlying layers flatten the steps of the alignment targets and cause alignment target reading problems by interfering with diffraction patterns formed by the alignment targets. See Jang col. 2, ll. 13-22. Thus, Jang is directed to providing a readable alignment mark by removing layers over an alignment mark area using a chemical-mechanical polishing (CMP) process. Jang describes providing a plurality of alignment mark trenches 48 in

an alignment mark area 30 of a semiconductor substrate 10. A pad oxide layer 42 and a silicon nitride layer 44 are formed sequentially above the plurality of alignment mark trenches 48 in at least the alignment mark area 30 of the semiconductor substrate 10. At least one isolation trench 43 is formed in the substrate 10 and an insulating layer 46 is formed at least over the alignment mark area 30. See Jang, col. 3, ll. 10-41 and Figure 2A. The insulating layer 46 is chemical-mechanically polished and the isolation trench 43 causes the chemical-mechanical polishing process to remove most (or all) of the insulating layer 46 from over the alignment mark trenches 48. See Jang, col. 3, ll. 42-55 and Figure 3B. The silicon nitride layer 44 and the pad oxide layer 42 are then removed over the alignment marks 48. See Jang, col. 7, ll. 4-10 and Figures 4-5.

However, Applicants respectfully submit that Jang fails to describe or suggest many features of the present invention. Jang is completely silent with regard to silicon-on-insulator technology and therefore does not teach or suggest forming a semiconducting layer positioned above the insulating layer. Instead, Jang describes forming a silicon nitride layer 44 above the pad oxide layer 42. Applicants respectfully submit that silicon nitride is an insulating material and not a semiconducting material. See, *e.g.*, "Silicon Processing for the VLSI Era," Volume 1: Process Technology, Second Edition, Stanley Wolf and Richard Tauber, Lattice Press, 2000, page 202 (copy attached). Thus, the silicon nitride layer 44 is not a semiconductor layer, as alleged by the Examiner at page 3 of the Office Action, but an insulator layer.

Applicants respectfully submit that Jang also fails to teach or suggest forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate. Instead, Jang describes forming an opening in the silicon nitride layer 44 and the pad oxide layer 42. Furthermore, Jang fails to describe or suggest forming a layer of material above the alignment mark and in the opening, *i.e.* the opening formed in the semiconducting layer and

the insulating layer. Thus, Applicants respectfully submit that claims 1-2 and 4-12 are not anticipated by Jang and request that the Examiner's rejections be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of Jang and Ridinger, either alone or in combination. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142.

As discussed in detail above, Jang fails to teach or suggest many of the limitations of the present invention. In particular, Jang fails to teach or suggest forming a semiconducting layer positioned above the insulating layer, forming an opening in the semiconducting layer and the

insulating layer to thereby expose a surface area of the bulk substrate or forming a layer of material above the alignment mark and in the opening.

Jang also fails to provide any motivation to modify the cited prior art to arrive at the claimed invention. As discussed above, Jang is completely silent with regard to silicon-on-insulator technology and therefore provides no motivation for forming a semiconducting layer positioned above the insulating layer or forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate. Moreover, Jang teaches away from at least some aspects of the present invention, *e.g.* forming a layer of material above the alignment mark and in the opening. In particular, Jang teaches that layers of material overlying the alignment marks may cause alignment target reading problems by interfering with the diffraction pattern produced by the alignment marks. Thus, Jang teaches a method of providing a readable alignment mark by removing layers over an alignment mark area. See Jang, col. 2, ll. 16-21.

For at least the aforementioned reasons, Jang does not achieve the advantages of the present invention, which may include preserving the integrity of the alignment mark throughout the processing life of the wafer and increasing the stability of the alignment marks. Moreover, through use of the present invention, it is believed that alignment procedures used in semiconductor manufacturing operations may be performed more accurately and reliably. As a result, manufacturing efficiencies and product yields may also increase. See Patent Application, page 14, ll. 6-18.

With particular regard to claim 3, the Examiner relies on Ridinger to teach a wafer diameter in a range of 3 to 6 inches. However, Ridinger does not remedy the aforementioned deficiencies of the primary reference. Thus, Applicants respectfully submit that claim 3 is not

obvious over Jang in view of Ridinger and request that the Examiner's rejection of claim 3 be withdrawn.

With regard to the new claims 44-59, Applicants respectfully submit that claims 44-46 depend from independent claim 1 and are therefore are allowable over the cited prior art for at least the aforementioned reasons. With particular regard to new independent claim 47, Applicants describe and claim providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. Applicants also describe and claim forming an opening in the semiconducting layer and the insulating layer to thereby expose an unpatterned surface area of the bulk substrate, forming an alignment mark in the bulk substrate within the exposed unpatterned surface area of the bulk substrate, and forming a layer of material above the alignment mark and in the opening. Thus, for at least the aforementioned reasons, Applicants respectfully submit that claims 47-59 are allowable over the cited prior art.

For at least the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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